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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: To be assigned
Examiner: To be assigned

In Re PATENT APPLICATION Of:

Applicants : Norio TAKAHASHI)

Appln. No. : 10/775, 232)

Filed : February 11, 2004)

For : MODULE CIRCUIT BOARD FOR)
SEMICONDUCTOR DEVICE)
HAVING BARRIERS TO ISOLATE)
I/O TERMINALS FROM SOLDER)

Attorney Ref. : F97ED0740-DIV3)

INFORMATION
DISCLOSURE
STATEMENT

September 15, 2004

Sir:

This is an information disclosure statement submitted in compliance with the timing requirements of 37 C.F.R. §1.97(b)(3).

Attached is one Japanese laid-open patent publication. English abstract and translation is attached hereto. The publication is listed on the attached Form PTO-1449. Should any fee be needed, please charge it to our Account No. 50-0945 and advise us accordingly.

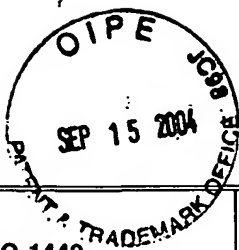
Consideration of the submitted document is respectfully requested.

Respectfully submitted,



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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

Atty Docket

F97ED0740-DIV3

U.S. Application No.:

10/775,232

Applicant

Norio TAKAHASHI

U.S. Filing Date: February 11, 2004

Group

To be assigned

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

		Document Number	Public Date	Country	Class	Sub-Class	Translation
	AM	Laid open P9-64503	08/21/95	JAPAN	H05K	1/14	Abstract and Translation
	AN						
	AO						
	AP						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	
	AS	

Examiner

Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.